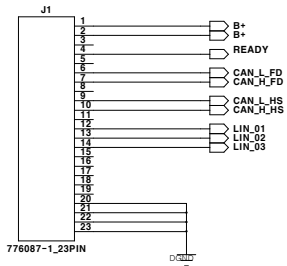


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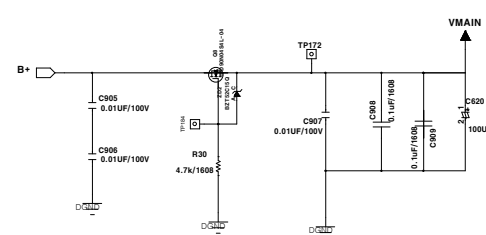
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2	CSI Interface	NO Connection	1	NOTE
3	MMC Interface	NO Connection	1	NOTE
4	SERDES	NO Connection	1	NOTE
5	UFS Interface	NO Connection	1	NOTE
6	LPDDR4	NO Connection	2	NOTE
7	EMIF	NO Connection	2	NOTE
8	MCU FLASH	NO Connection	2	NOTE
9	OSPI FLASH	NO Connection	3	NOTE
10	HYPER FLASH+HYPER RAM	NO Connection	3	NOTE
11	MCU & MAIN GENERAL I/O, OSC CLK/SNO Connection		1	NOTE
12	CSI Interface	NO Connection	1	NOTE
13	MMC Interface	NO Connection	1	NOTE
14	SERDES	NO Connection	1	NOTE
15	UFS Interface	NO Connection	1	NOTE
16	LPDDR4	NO Connection	2	NOTE
17	EMIF	NO Connection	2	NOTE
18	MCU FLASH	NO Connection	2	NOTE
19	OSPI FLASH	NO Connection	2	NOTE
20	HYPER FLASH+HYPER RAM	NO Connection	2	NOTE

		<div style="text-align: center;"> <h1>UNICK</h1> </div>		A
		<div style="text-align: center;"> <h2>Title</h2> <h1>AI 기반 공조제어기</h1> <h3>00_PAGE_LIST</h3> </div>		
Project No.				
Drawn		Drawing number		A1
Checked		File name		
Released		<div style="text-align: center;"> 시기반공조제어기원로도_VER0038 </div>	<div style="text-align: center;"> Rev. </div>	
Update	2025-02-20	PCB filename	Sheet 1 of 17	<div style="text-align: center;"> A Sample </div>
		<div style="text-align: right;"> 제작 _250220.sch </div>		

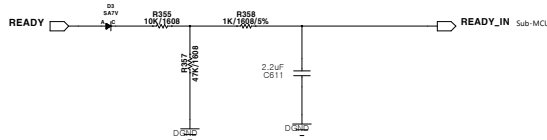
MAIN CONNECTOR (Ext)



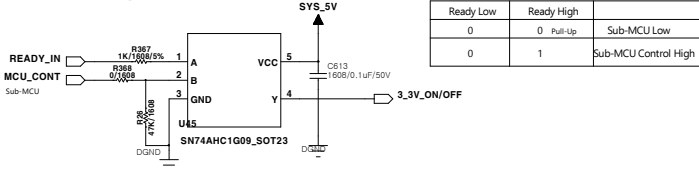
Protection Circuit



Ready Signal



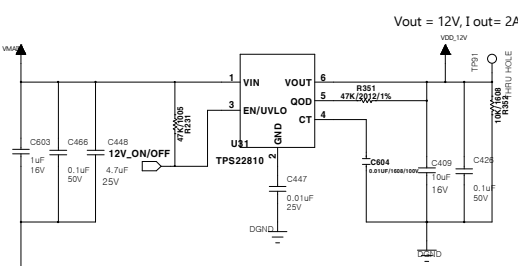
3.3V Regulator Control



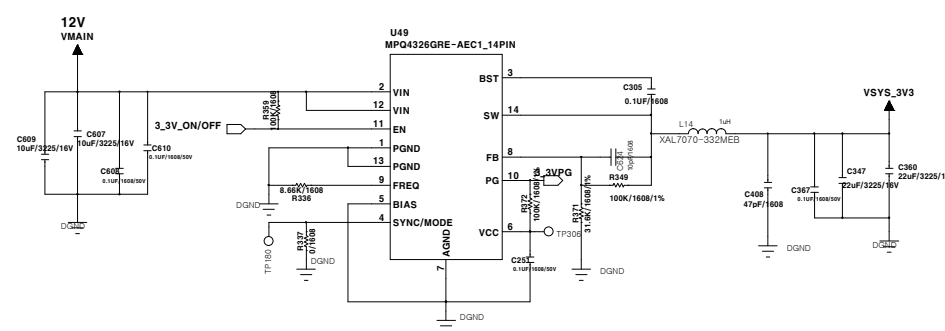
3.3V Regulator Control Truth Table(And Gate)

Ready Low	Ready High	
0	0	Sub-MCU Low
0	1	Sub-MCU Control High

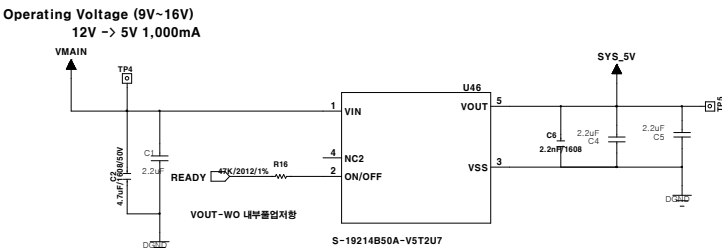
Load Switch (Main -> VDD_12V)



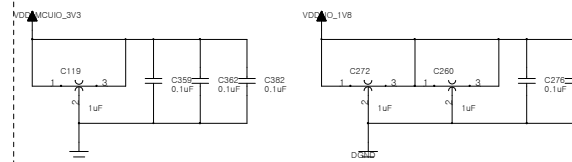
DC-DC (Main -> VDD_3V3)



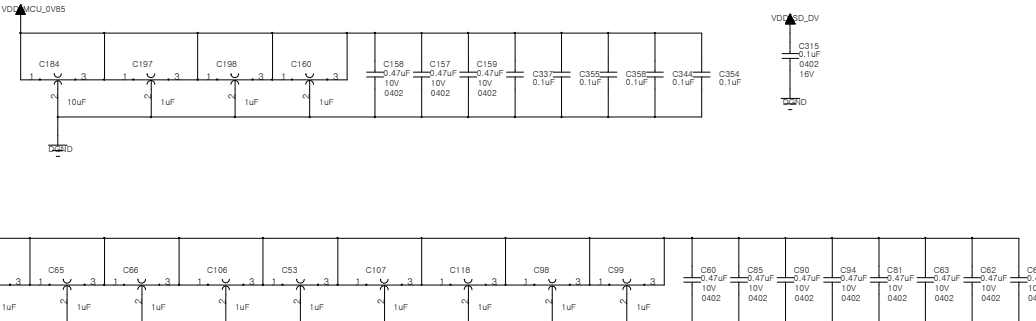
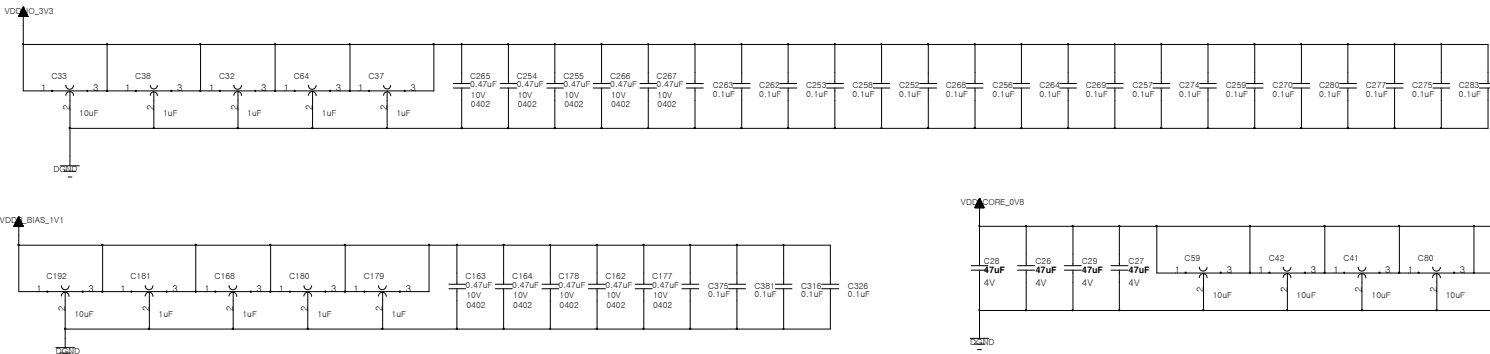
LDO (Main -> VDD_5V)



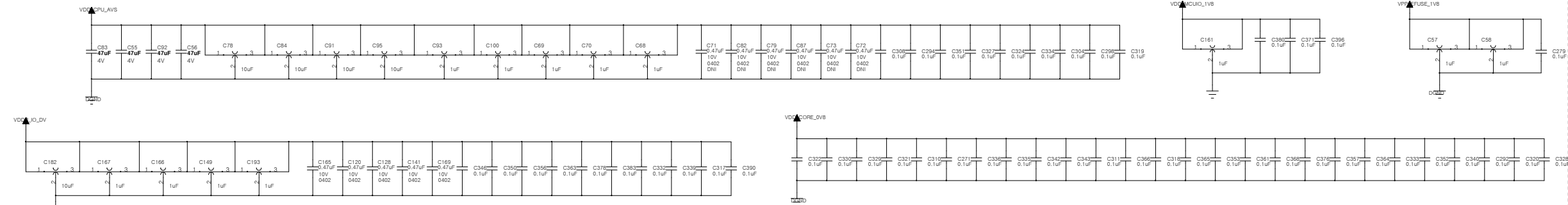
CPU_Bypass_3



CPU_Bypass_1



CPU_Bypass_3



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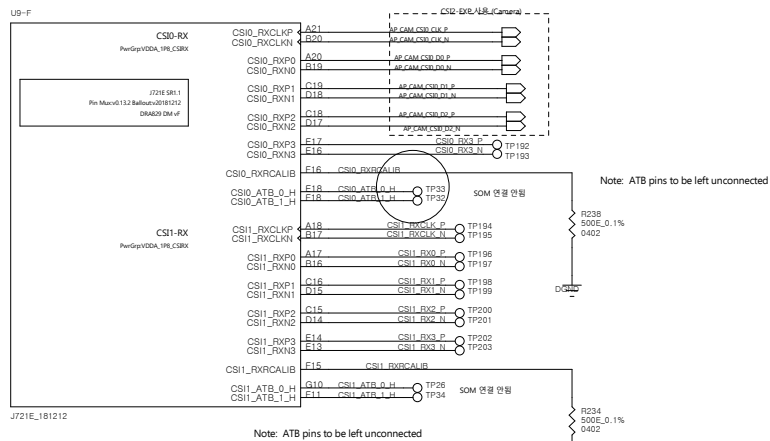
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A141	VSS	VSS	VSS
A142			

The diagram illustrates the power and digital architecture of the J721E-1B1212 board. Key components and connections include:

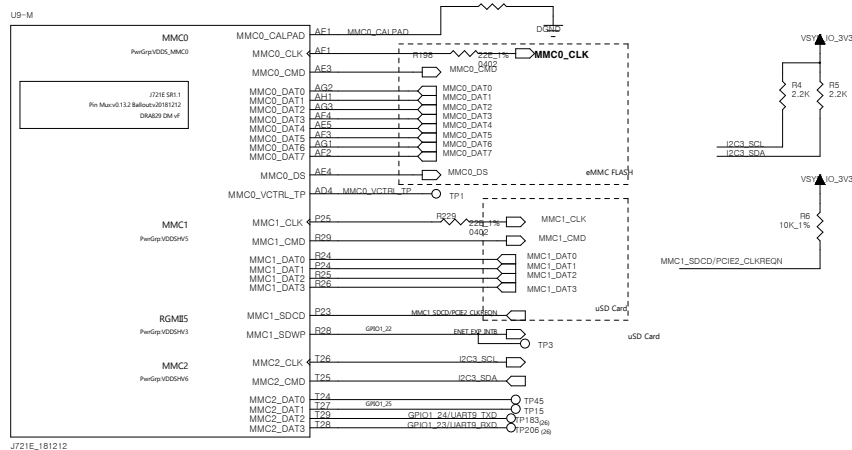
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Project No.		Title	
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Checked		AI 기반 공조제어기	
Released		02_CPU_POWER	
Update		Drawing number	
2025-02-20		Size	
PCB filename		A1	
File name		Rev.	
A1기반공조제어기회로도_VER038		3 of 17	
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CSI Interface



MMC Interface



Via Probe Test Points

Place Near SOC

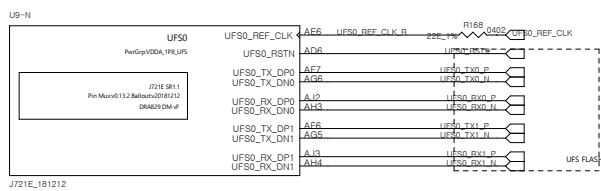
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MMC0_DATA3	TP20_SMD	TP53
MMC0_DATA4	TP20_SMD	TP55
MMC0_DATA5	TP20_SMD	TP51
MMC0_DATA6	TP20_SMD	TP47
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MMC0_DS	TP20_SMD	TP56
MMC0_CMD	TP20_SMD	TP54

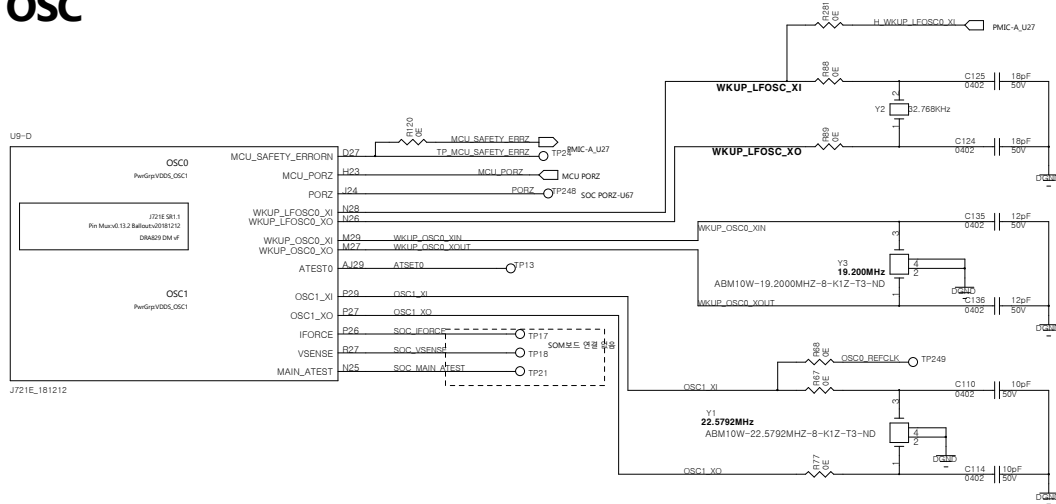
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MMC1_DATA0	TP20_SMD	TP57
MMC1_DATA1	TP20_SMD	TP61
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MMC1_DATA3	TP20_SMD	TP59
MMC1_CMD	TP20_SMD	TP60

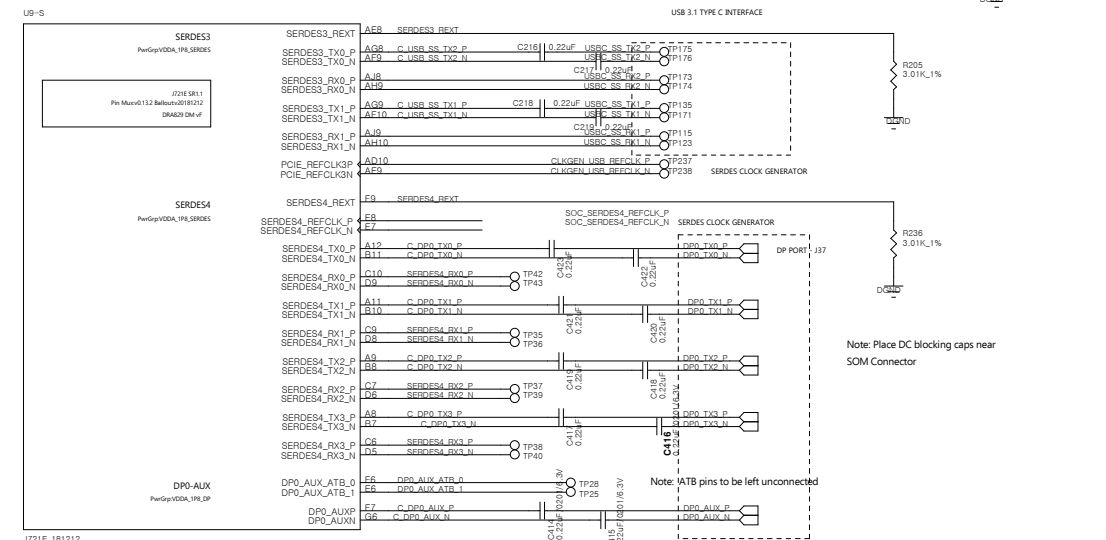
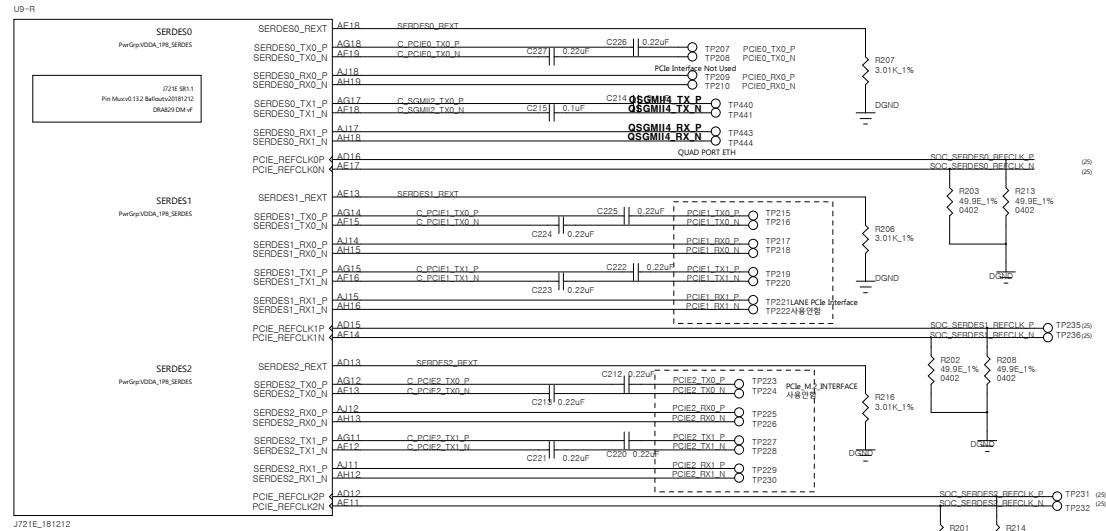
UFS Interface



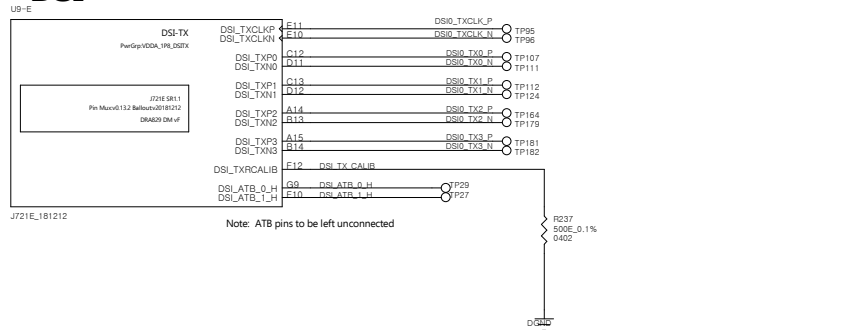
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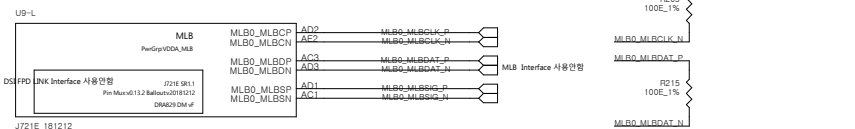
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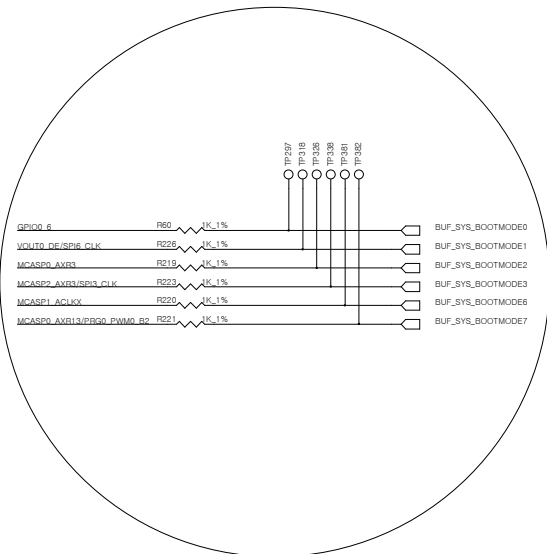


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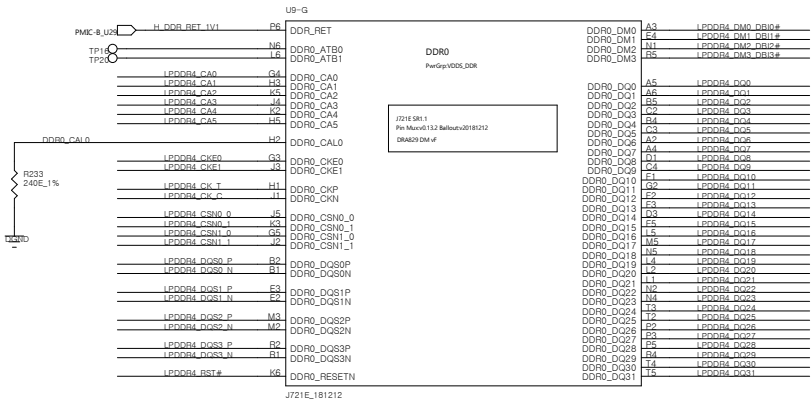


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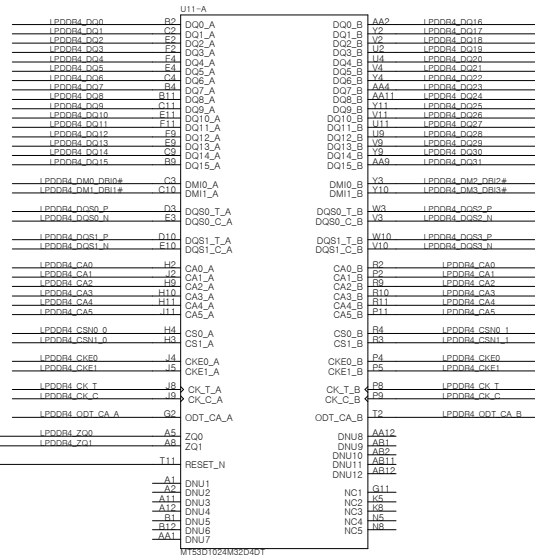


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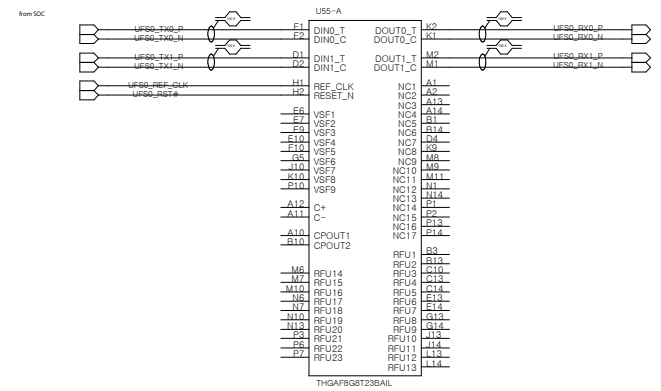
DDR4 Memory

EMIF

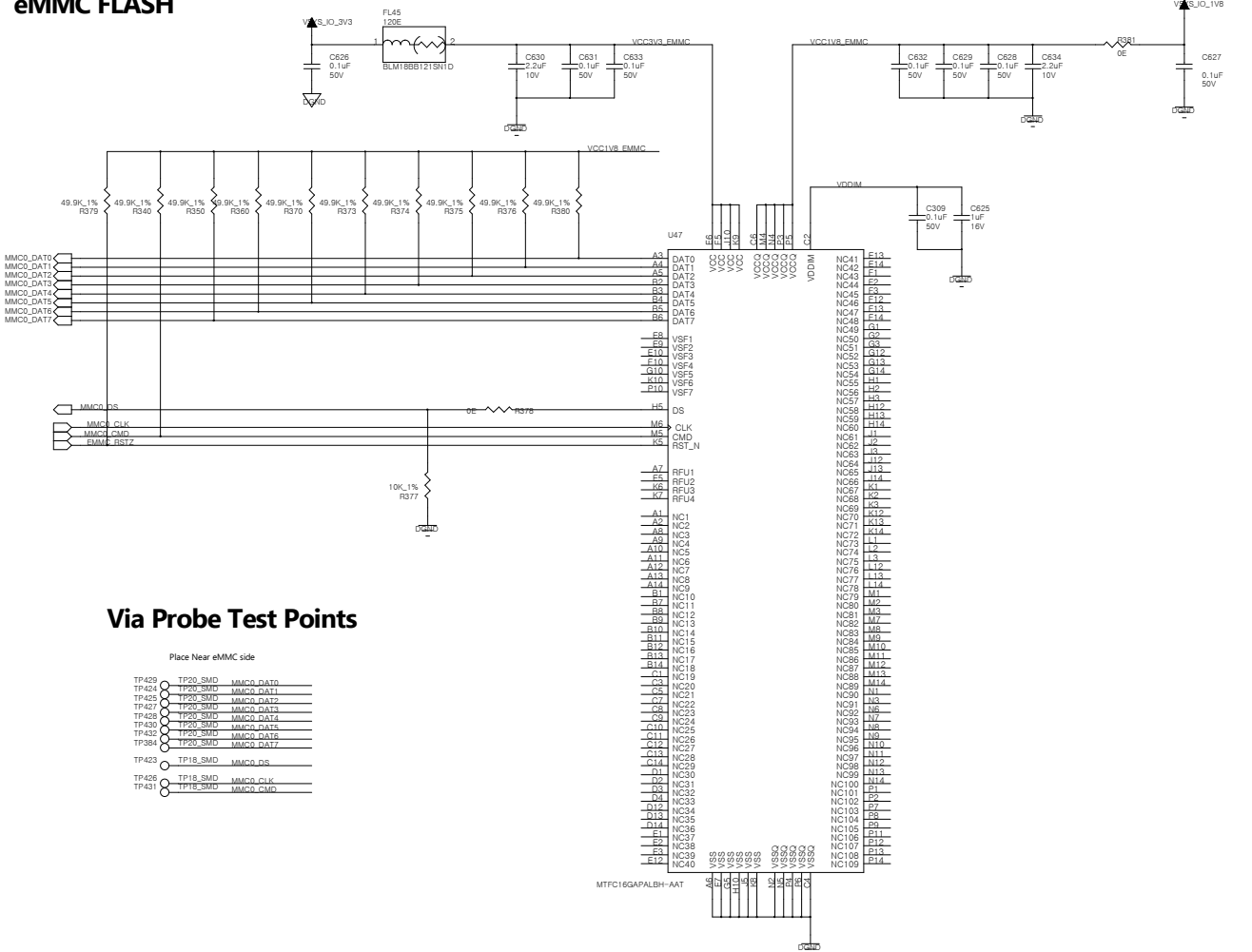
LPDDR4



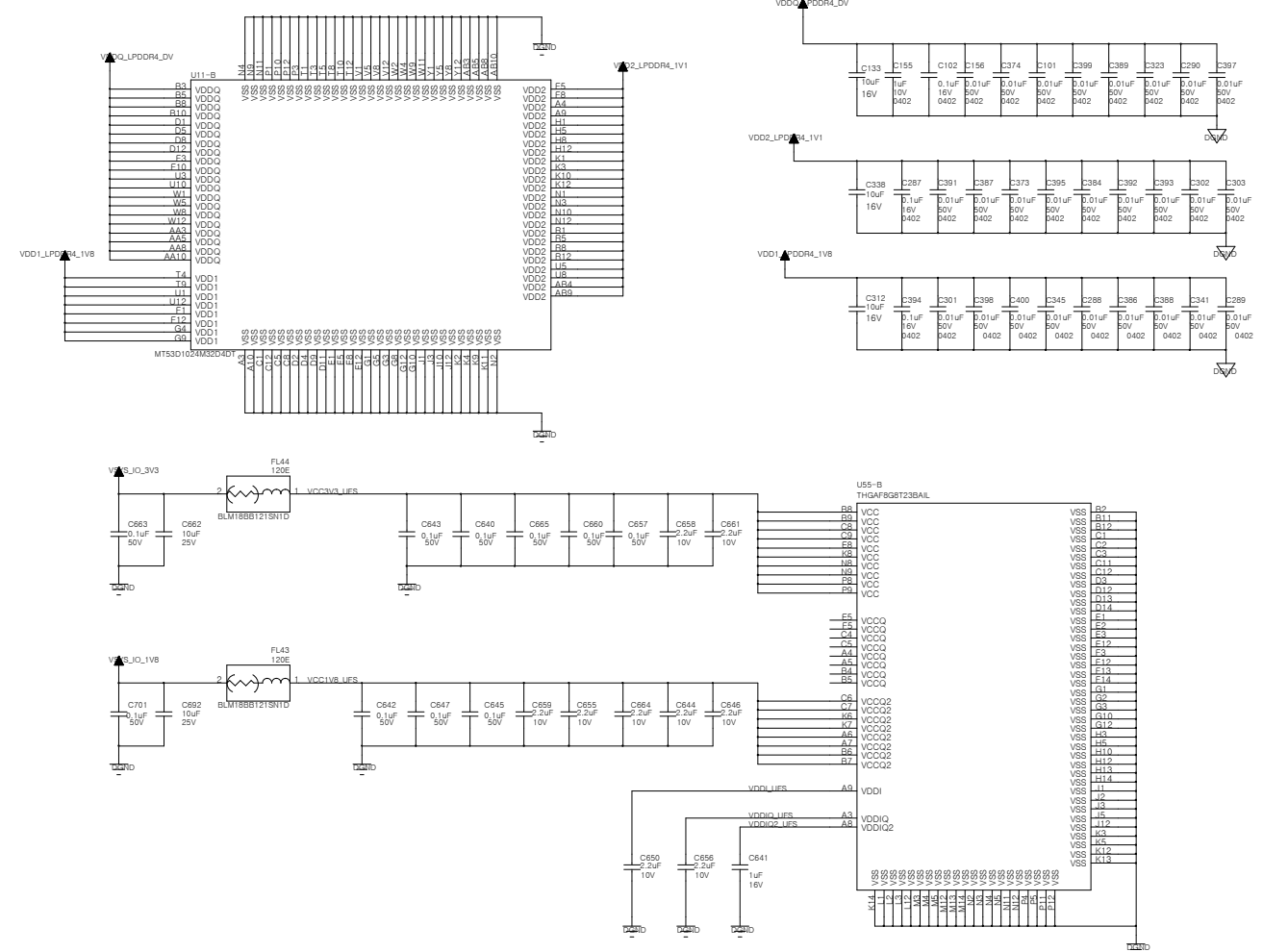
UFS FLASH



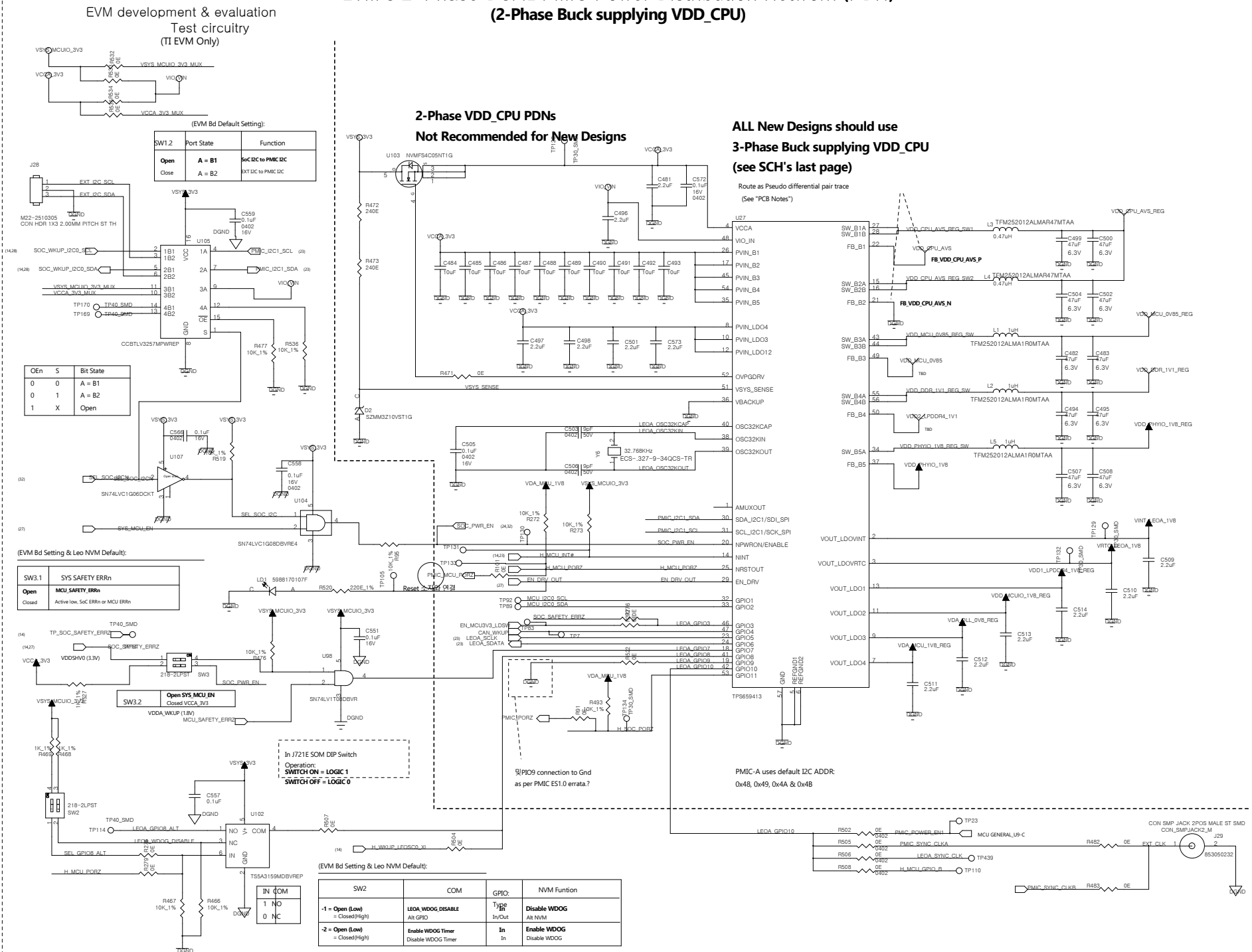
eMMC FLASH



Bypass_GND



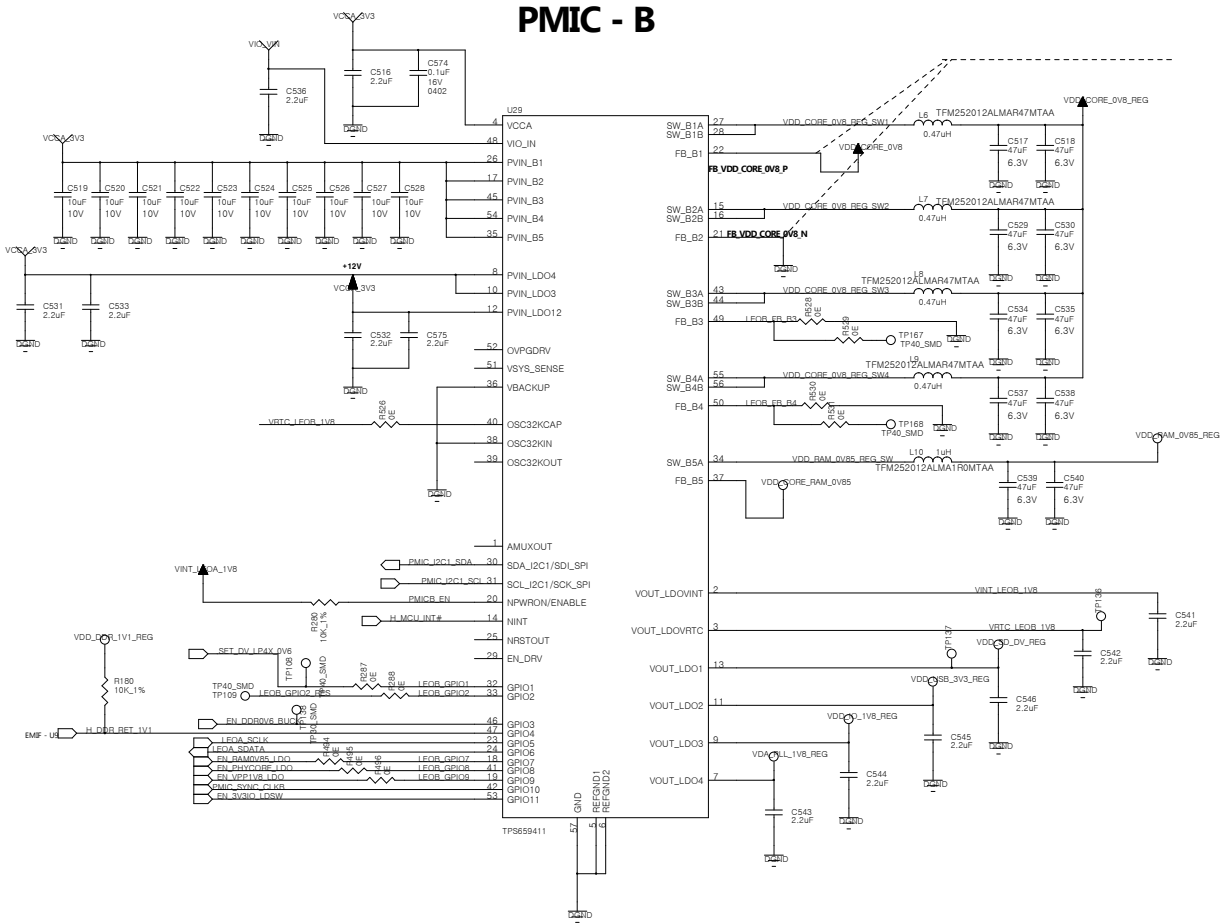
EVM's 2-Phase DUAL PMIC Power Distribution Network (PDN)
(2-Phase Buck supplying VDD_CPU)



2-Phase VDD_CPU PDNs
Not Recommended for New Designs

ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(see SCH's last page)

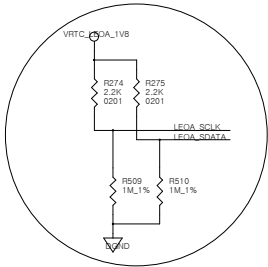
PMIC - B

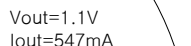
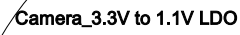
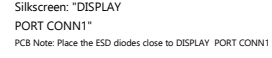


*PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

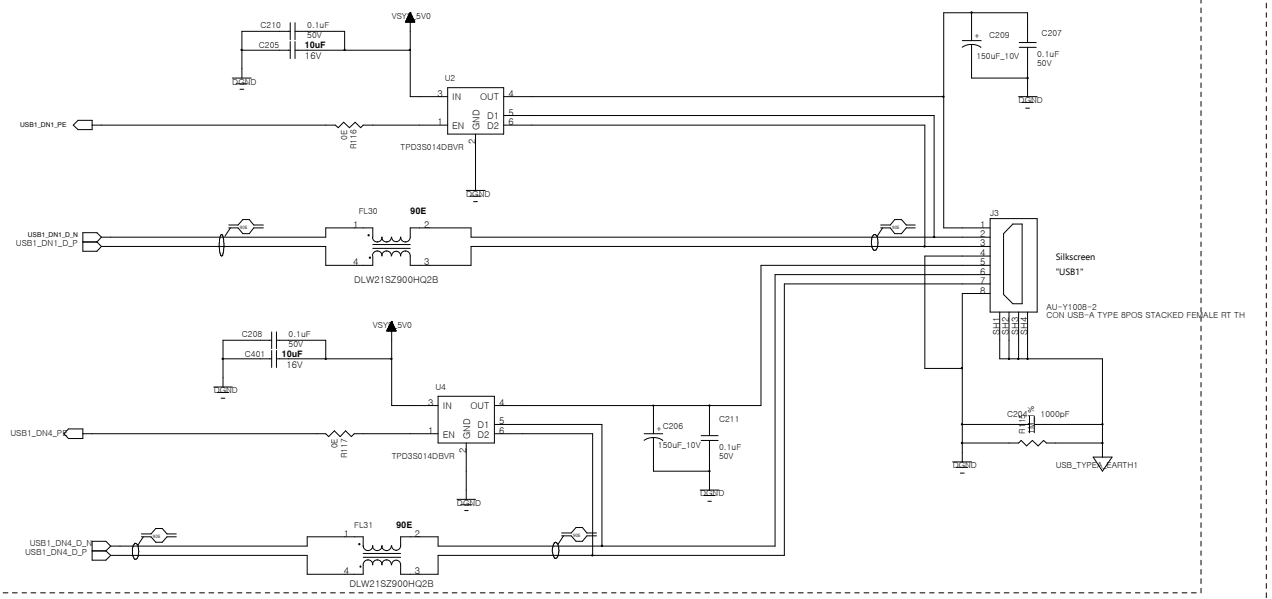
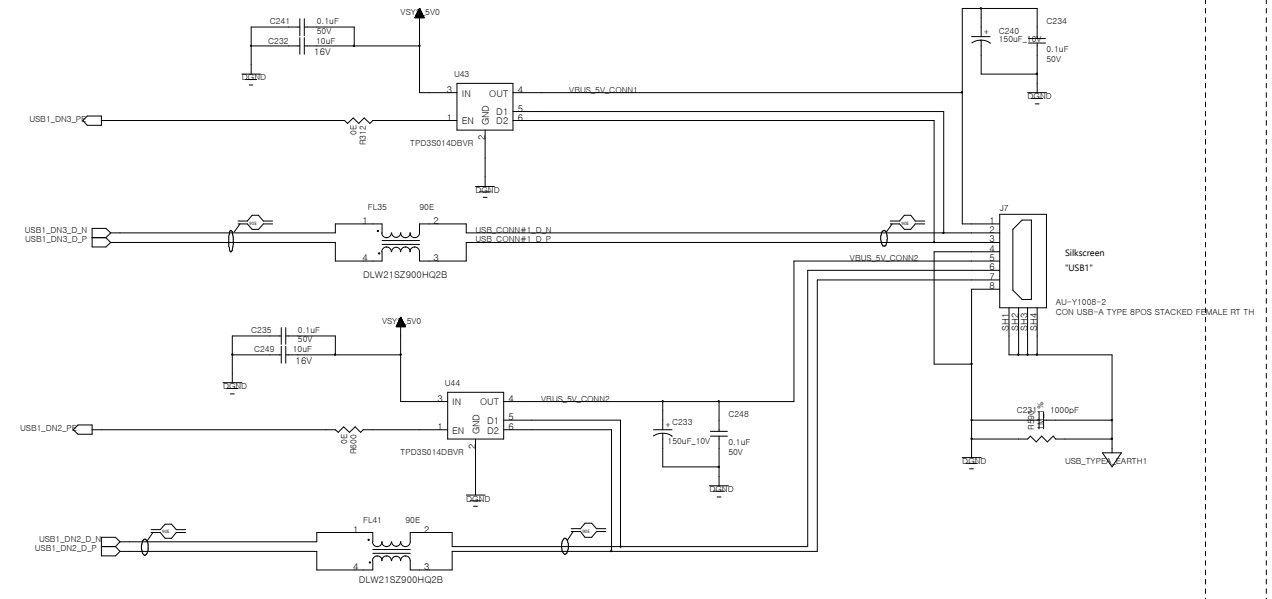
For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F



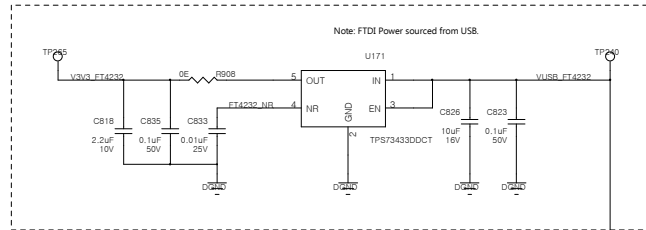


		<div>UNICK</div> <div>Title</div> <div>AI 기반 공조제어기</div> <div>10_IF_CAMERA</div>		A
Project No.		Drawing number	Size	
Drawn			A1	
Checked		File name	Reg.	
Released		시각기반공조제어기하물로드_VER038_A Sample	제각_250220.ach	
Update	2025-02-20	PCB filename	Sheet 9 of 17	

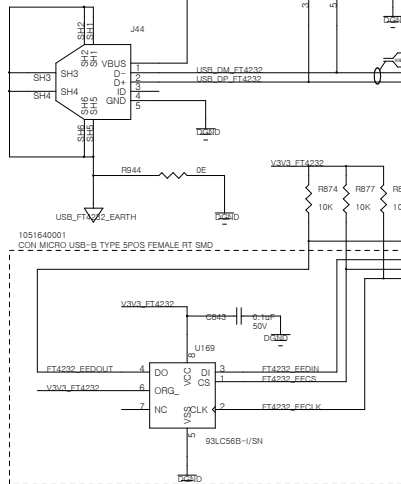
[illegible][illegible]

Project No.		Drawing number		Size	
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Checked		File name		Rev.	
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Update	2026-02-28	PCB filename	Sheet	10 of	17

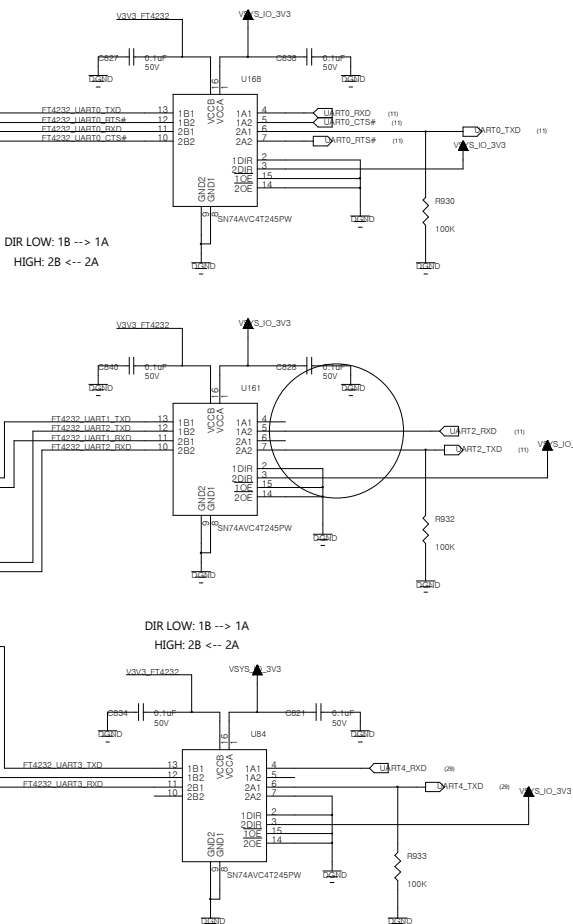
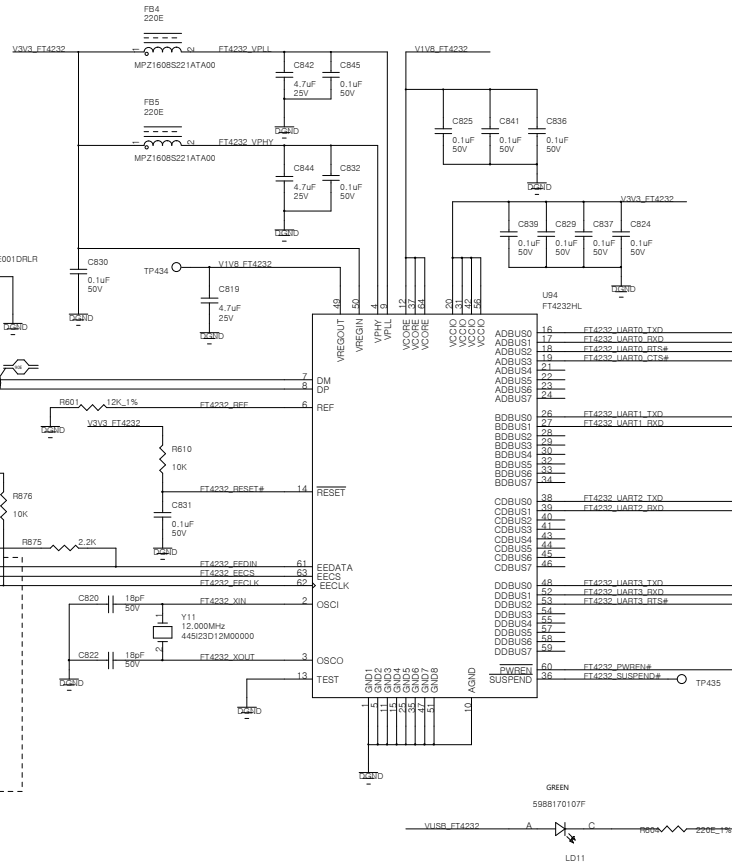
QUAD PORT FTDI



Silkscreen
"MAIN-UART"

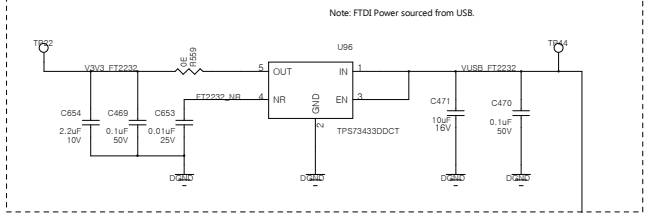


Note: FTDI EEPROM for storing manufacturing/configuration information.

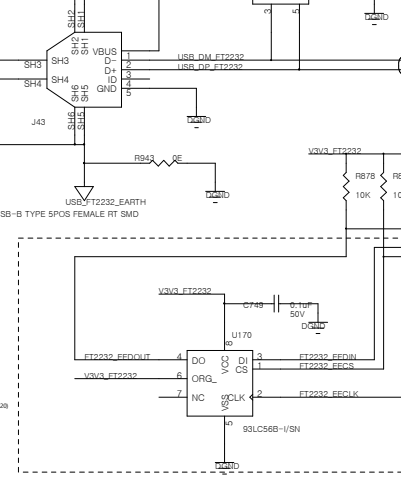


DIR LOW: 1B --> 1A
HIGH: 2B <-- 2A

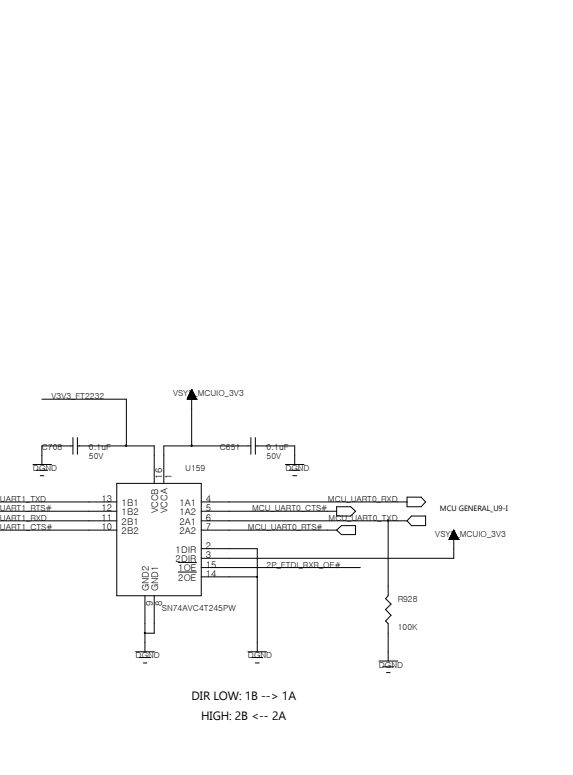
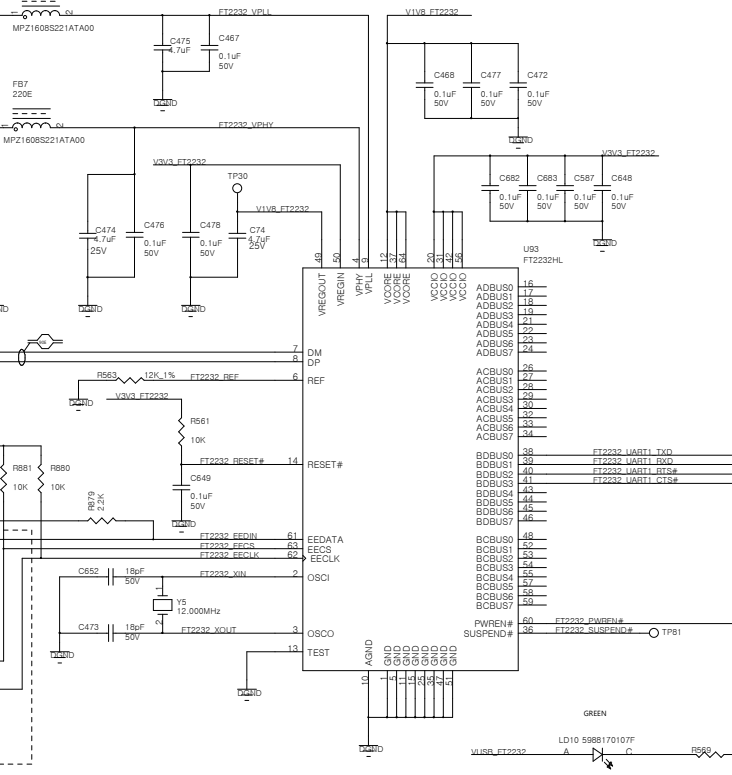
DUAL PORT FTDI



Silkscreen
"MCU-UART"

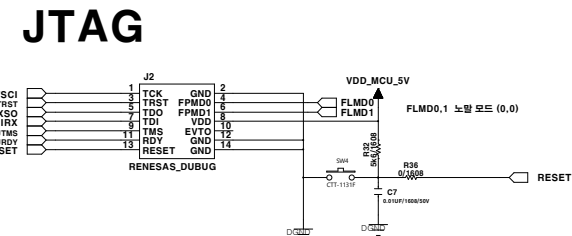
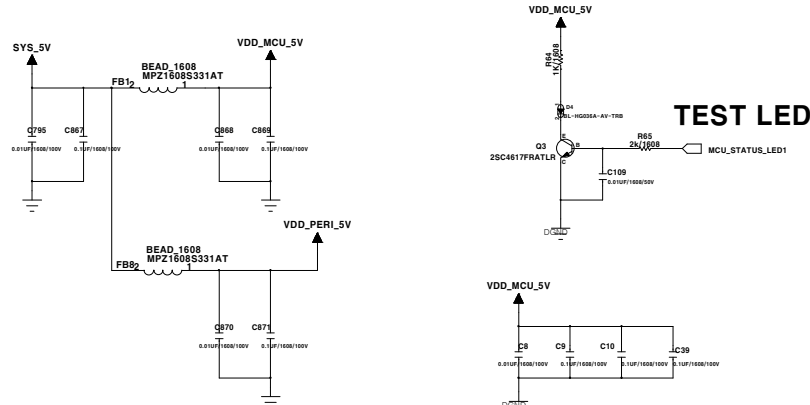
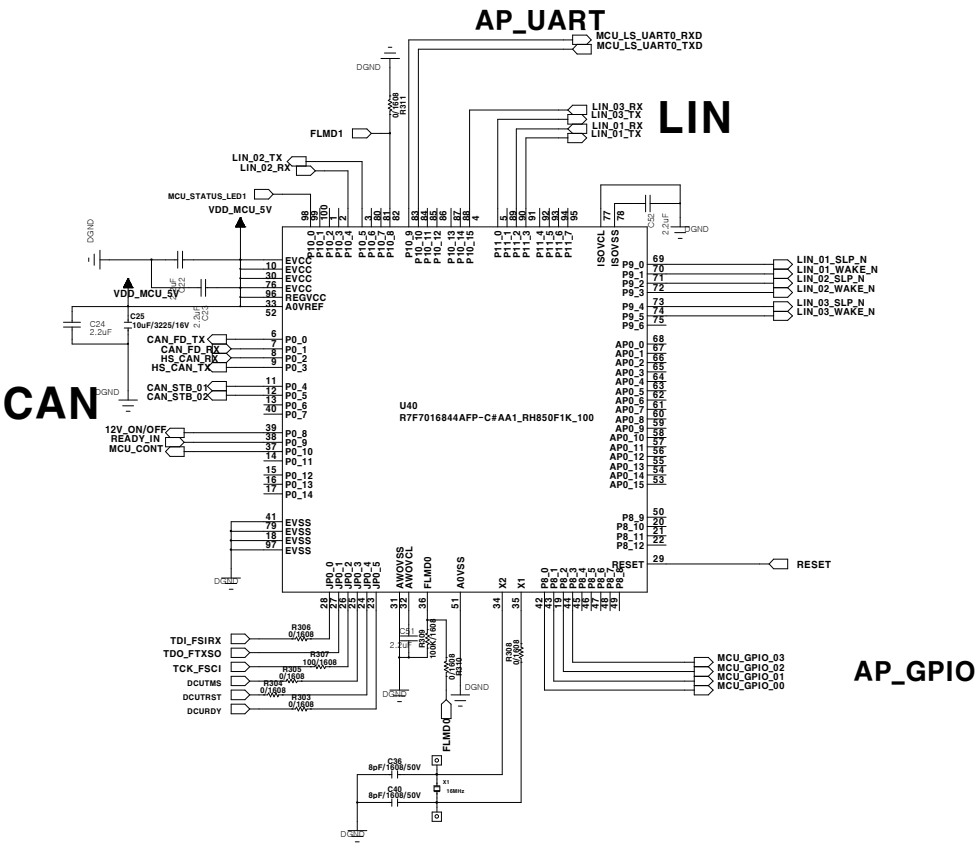


Note: FTDI EEPROM for storing manufacturing/configuration information.

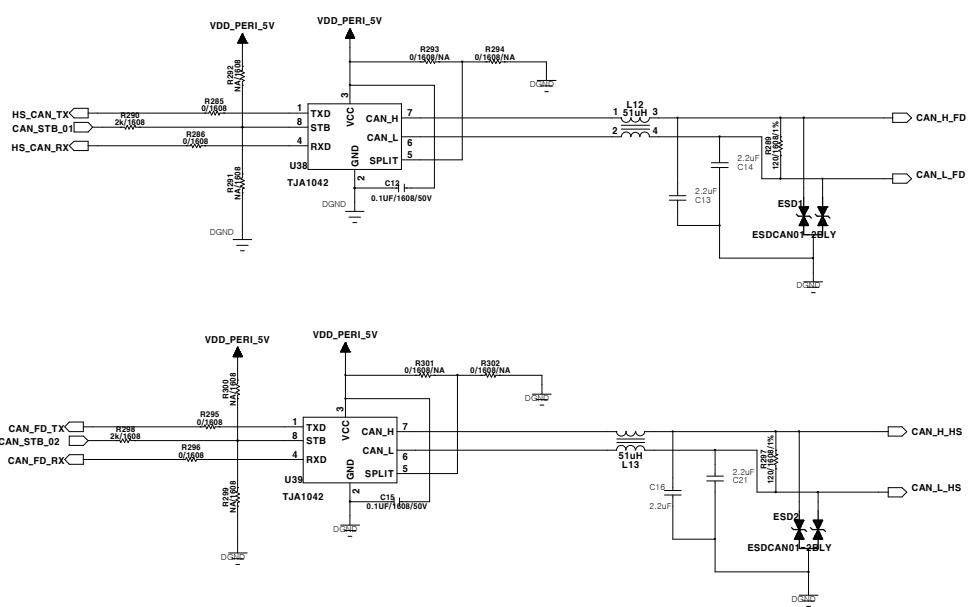


DIR LOW: 1B --> 1A
HIGH: 2B <-- 2A

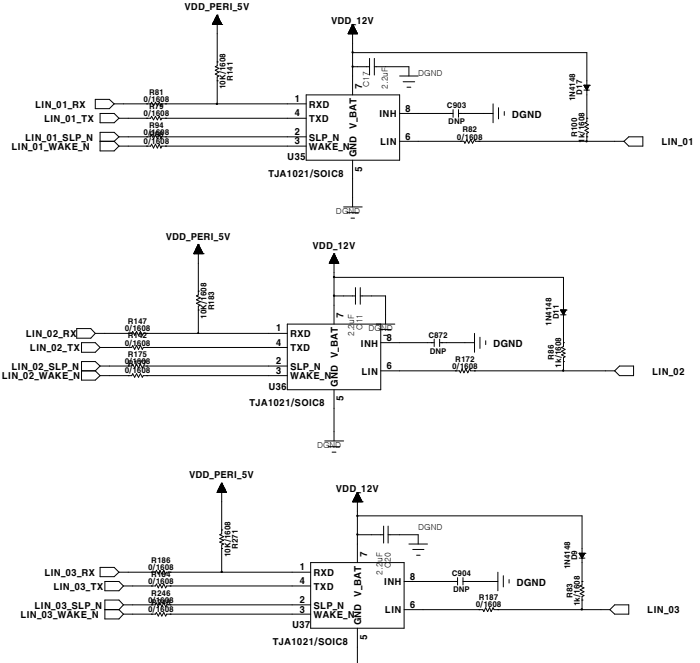
SUB MCU



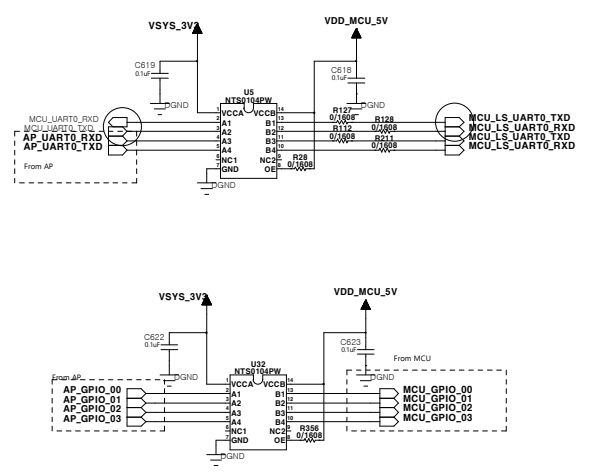
CAN-FD, HS-CAN Communication



LIN Communication



Level Shift Signal

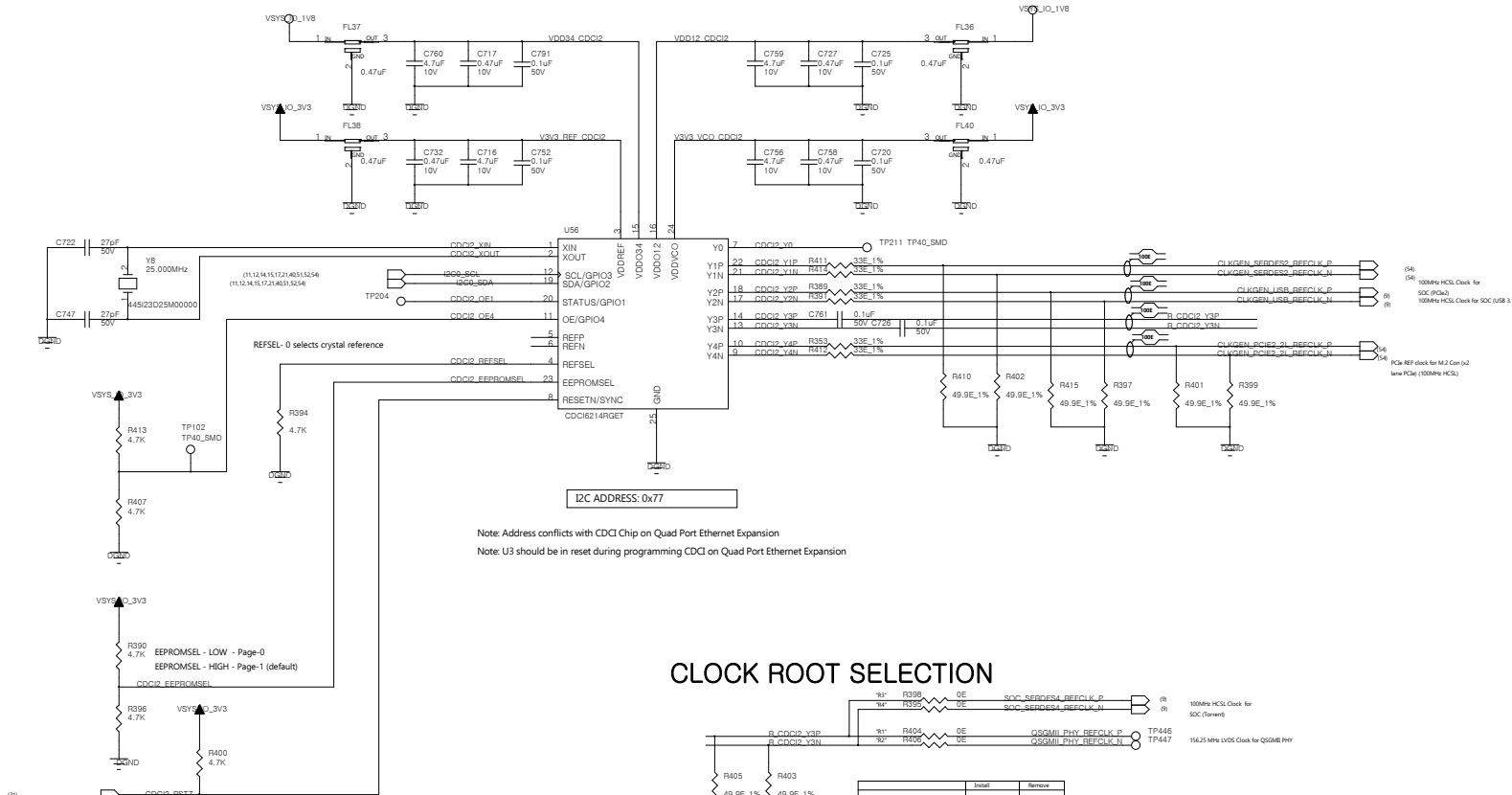


CONFIG DIP SWITCH

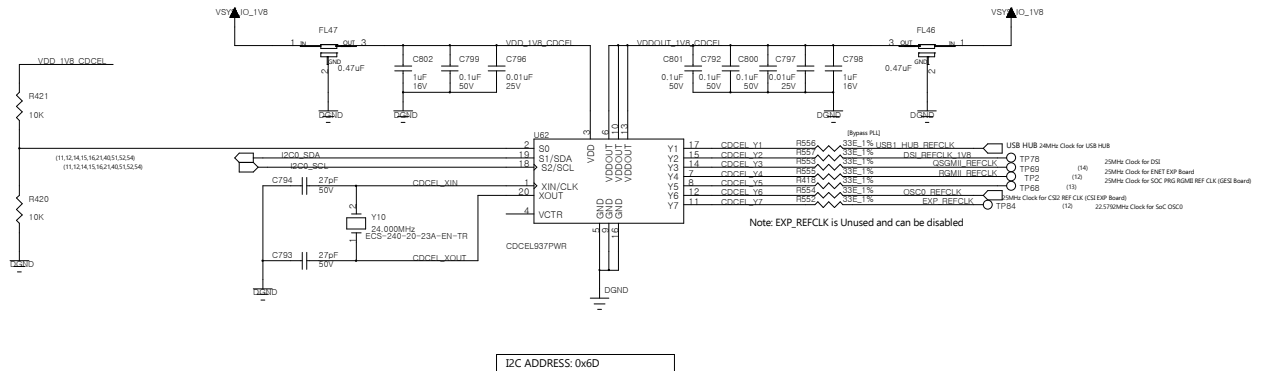


		<div>UNICK</div> <div>Title</div> <div>AI 기반 공조제어기</div> <div>17_RESET_BOTTOM</div>		A
Project No.		Drawing number	Size	
Drawn			A1	
Checked		File name	Rev	
Released		기기반공조제어기회로도_VER038_A Sample	0	제국_250220.sch
Update	2023-02-20	PCB filename	Sheet	13 of 17
		9		

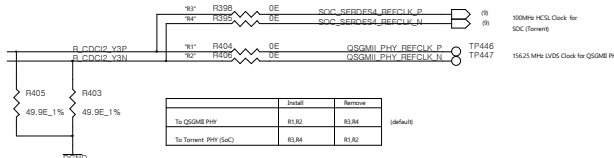
SERDES CLOCK GENERATOR #2



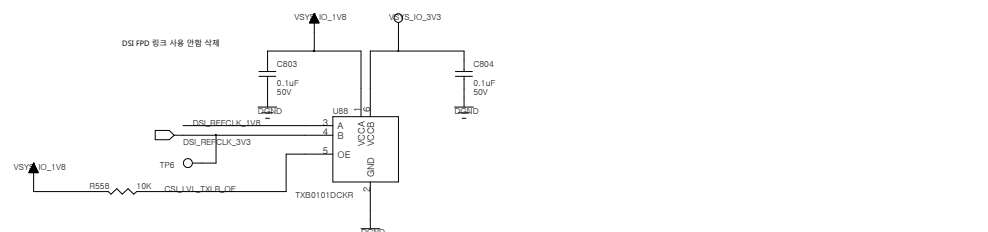
PERIPHERAL CLOCK GENERATOR



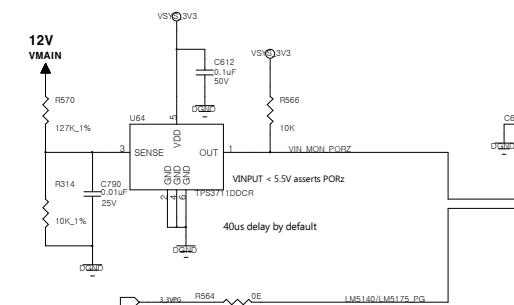
CLOCK ROOT SELECTION



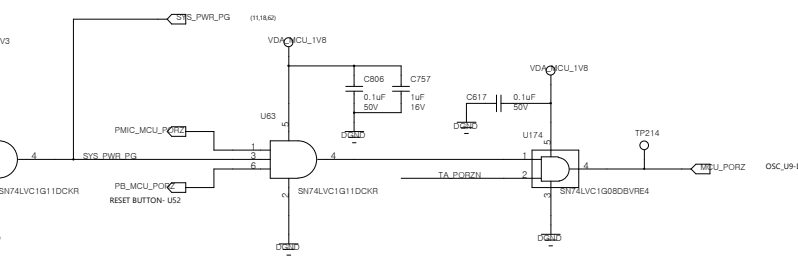
Level Translator for DSI REFCL



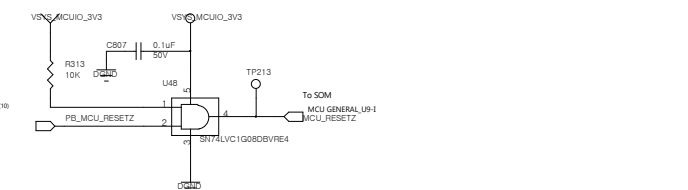
RESET INPUTS



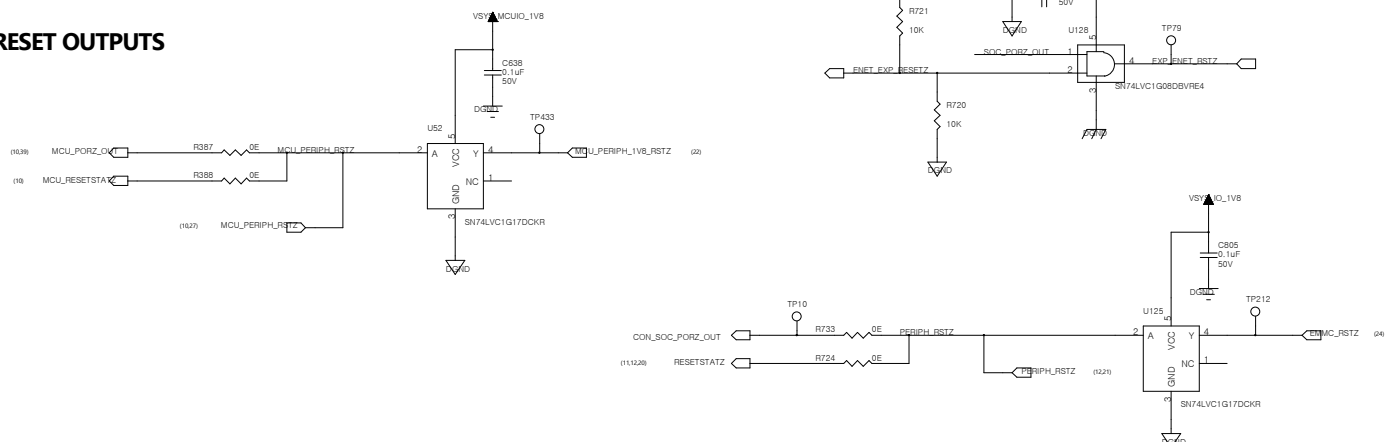
MCU PORT



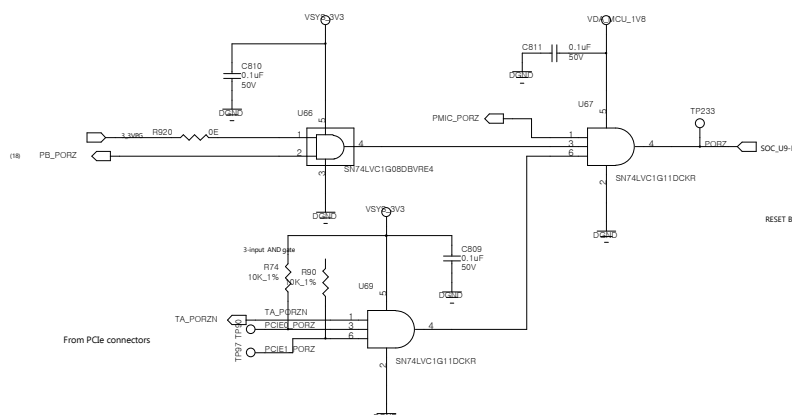
MCU RESE



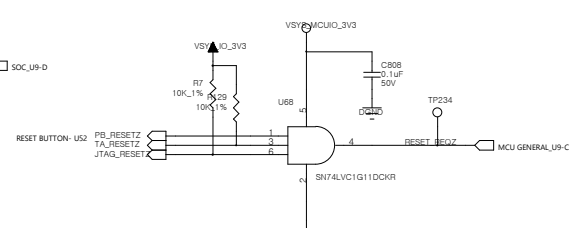
RESET OUTPUTS



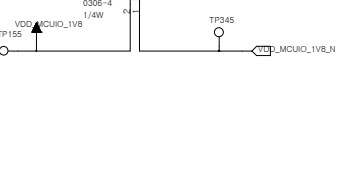
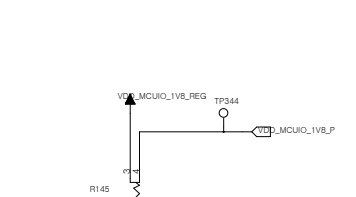
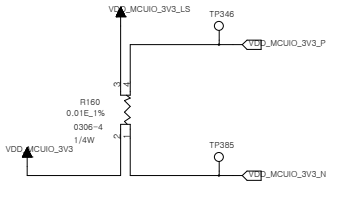
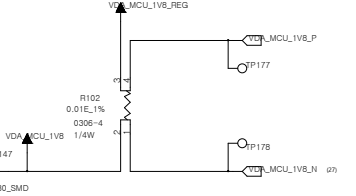
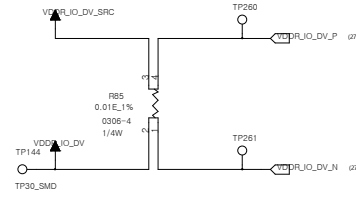
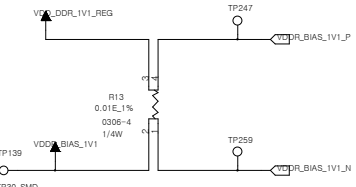
SOC POR



SOC RESE

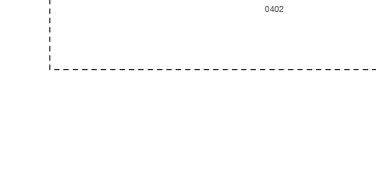
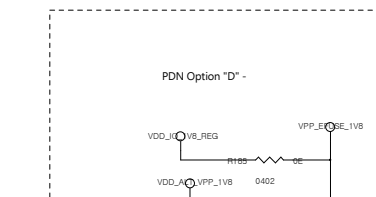
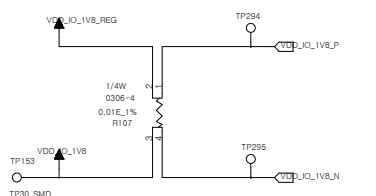
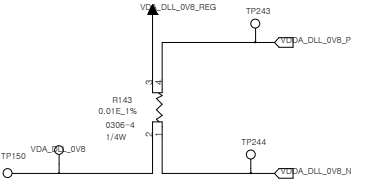
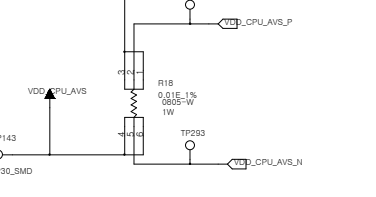
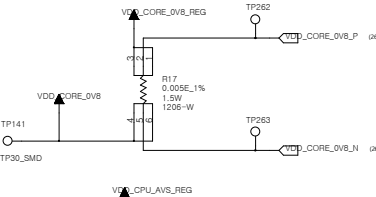
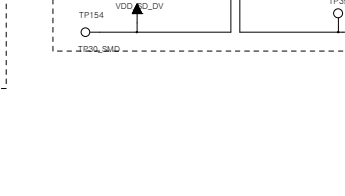
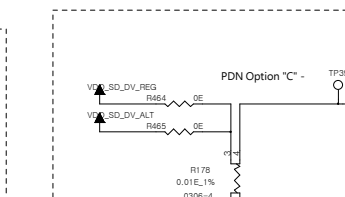
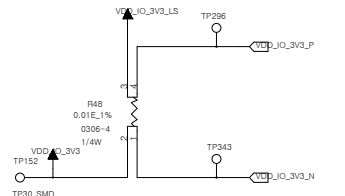
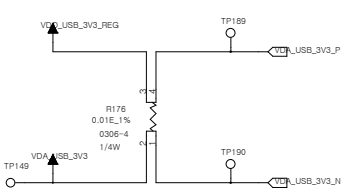
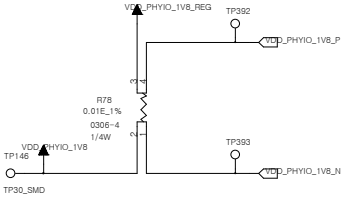
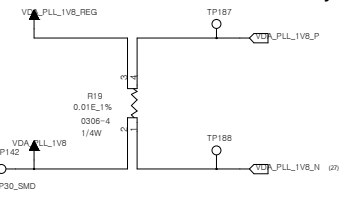


SOC Current Sense Resistors



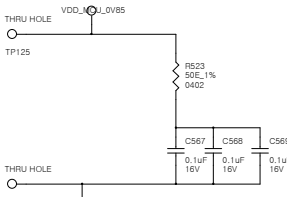
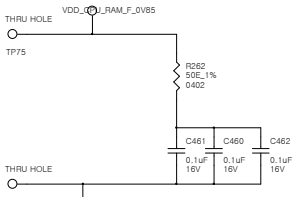
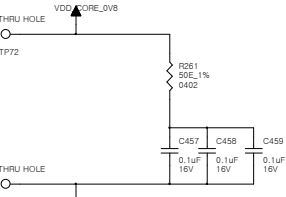
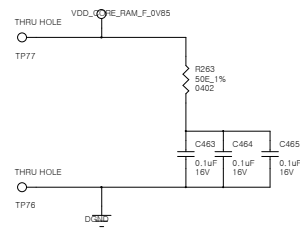
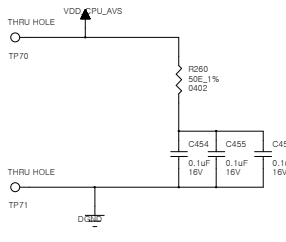
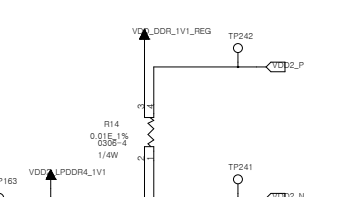
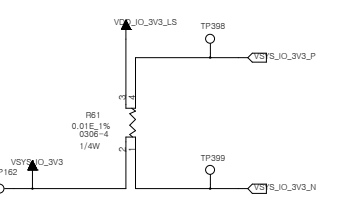
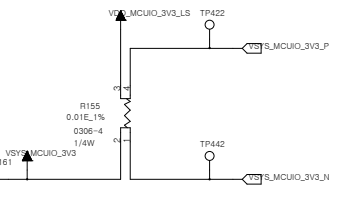
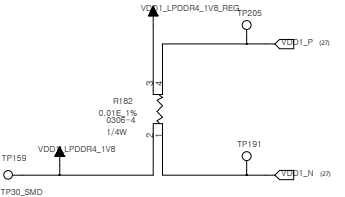
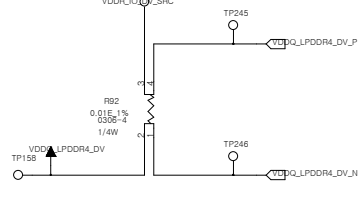
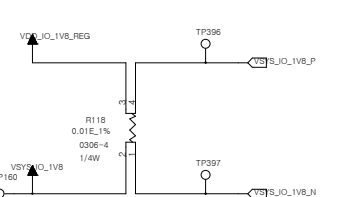
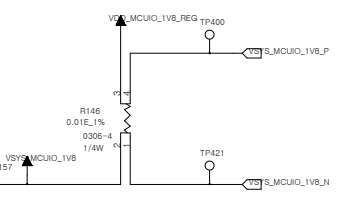
EVM development & evaluation test circuitry

(TI EVM Only)



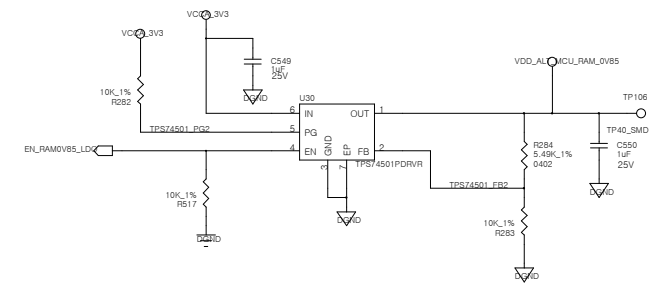
Supply Rail Kelvin Sensing

Peripheral Current Sense Resistors

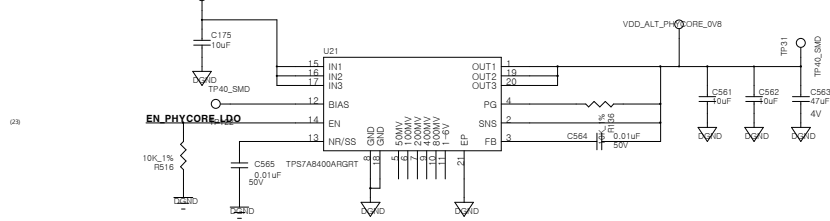


<div>Project No.</div> <div>Drawn</div> <div>Checked</div> <div>Released</div> <div>Validated</div>		<div>Title</div> <div>UNICK</div>		A
		<div>AI 기반 공조제어기</div> <div>20_CURRENT_SENSE_RES</div>		
<div>Drawing number</div> <div></div>		<div>Size</div> <div>A1</div>		<div>파일명_250220.acd</div>
<div>File name</div> <div>시각기반공조제어기필로드_VEP038_A Sample</div>		<div>Rev</div> <div>1 of 17</div>		
<div>PCN filename</div> <div>2025-02-20</div>		<div>Sheet</div> <div>1 of 17</div>		

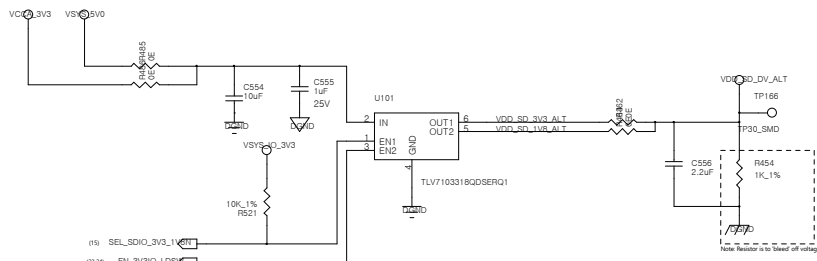
PDN Option ?A: VDD_MCU_RAM_0V85_ALT rail꺾 source



PDN Option ?B: VDD_PHYCORE_0V8_ALT rail꺾 source

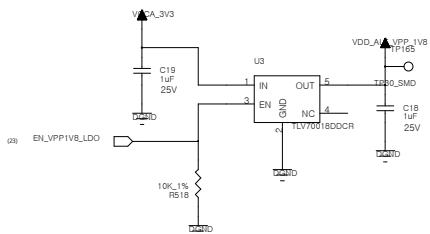


PDN Option ?C: VDD_SD_DV_ALT rail꺾 source



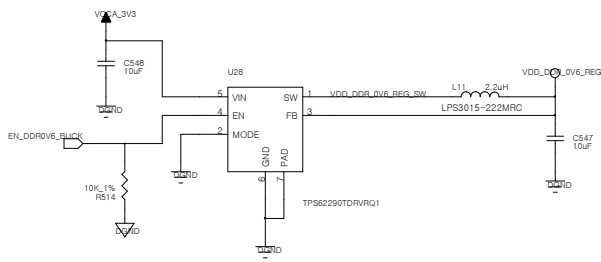
VDD_SD_DV_ALT	EN1	EN2	Comments
3.3V	HIGH	HIGH	Both enables driven high during power up seq to support initial 3.3V signaling per SD card protocol
1.8V	LOW	HIGH	SW controls & transition Sd card to high speed 1.8V signaling if card type supports

PDN Option ?D: VDD_VPP_1V8_ALT rail꺾 source

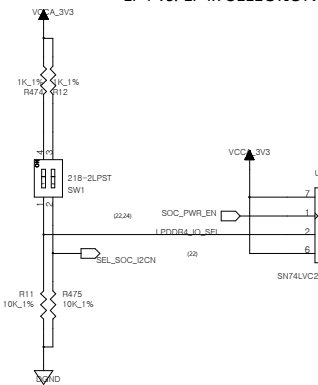


ALTERNATE LPDDR4X POWER SUPPLY OPTION

0.6V BUCK CONVERTER



LP4 vs. LP4x SELECTION



SW1

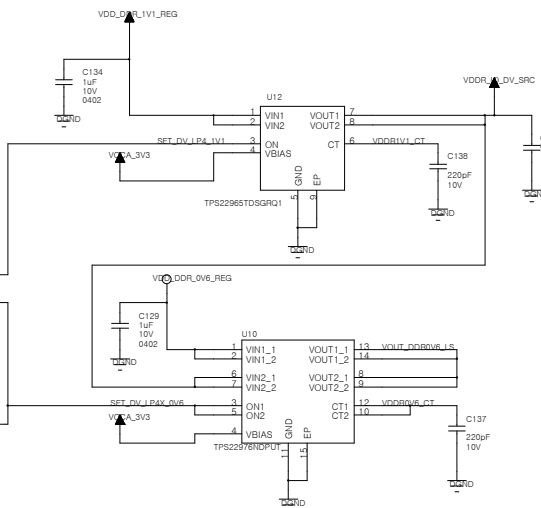
Pos1 - ON/High = LPDDR4 (default)

OFF/Low = LPDDR4x (optional)

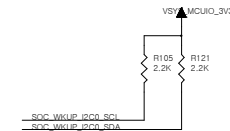
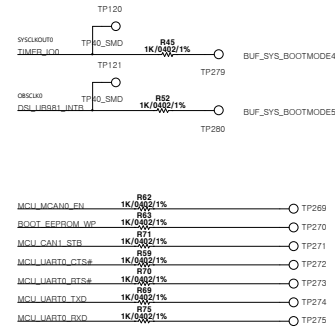
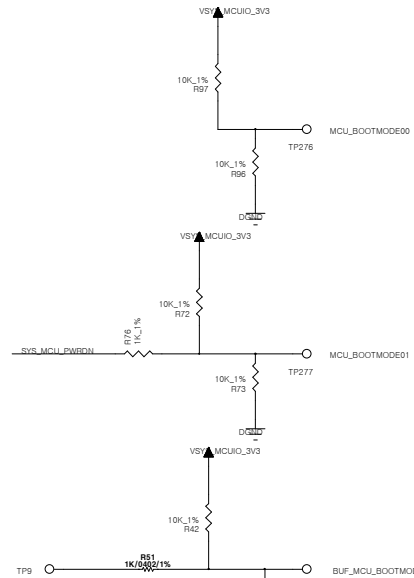
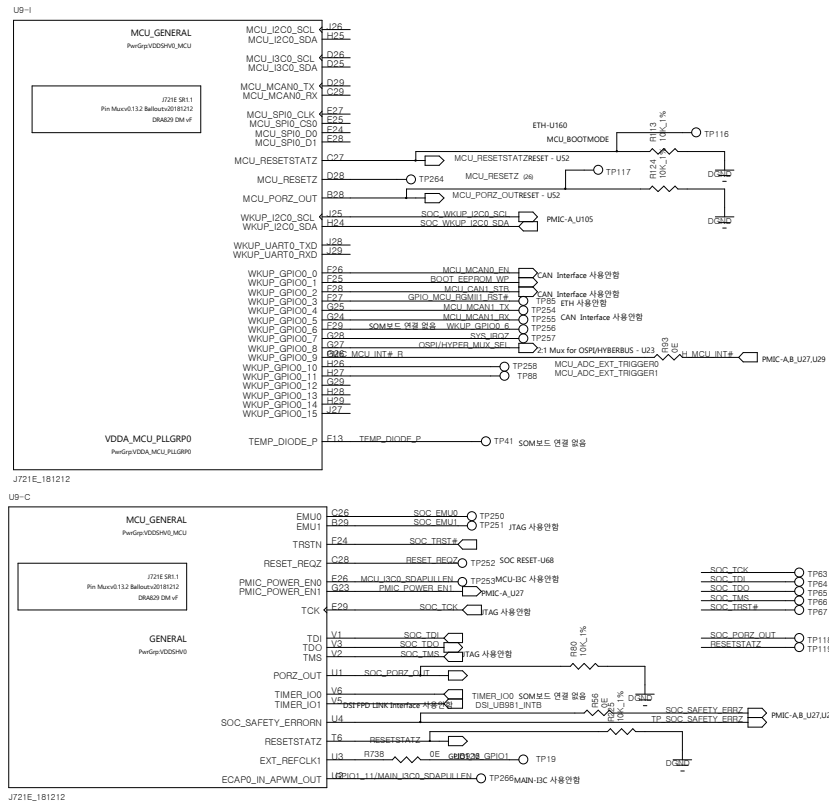
Pos2 - ON/High = PMIC I2C to Ext header I2C (optional)

OFF/Low = PMIC I2C to SoC WKUP I2C (default)

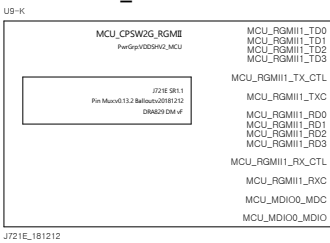
LP4 vs. LP4x VIO ISOLATION



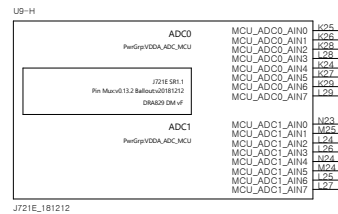
MCU & MAIN GENERAL IO, OSC CLKS



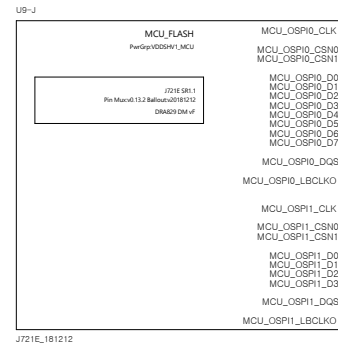
MCU_RGMII



MCU ADCs



MCU FLASH



		<div style="text-align: center;"> <h1>UNICK</h1> </div>		A
		<div style="text-align: center;"> <h2>Title AI 기반 공조제어기</h2> <h3>05_CPU_MCU_EXT</h3> </div>		
Project No.		<div style="display: flex; justify-content: space-between;"> <div> Drawing number File name A[기반공조제어기]하로드_VER038_A Sample </div> <div> Size A1 Rev. 제약_250220.sch </div> </div>		
Drawn				
Checked				
Released				
Update	2025-02-20	PCB filename	Sheet 17 of 17	